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Specification and Drawings, as originally filed, with Application for Patent Serial No: **2,474,111,** on July 8, 2004, by **GORDON JOHN ALLAN,** for "Method and Apparatus for Mixed-Signal DLL/PLL as Usefull in Timing Manipulation."

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ABSTRACT: MIXED-SIGNAL DLL/PLL FOR CLOCK ALIGNMENT AND MULTIPLICATION

The delay of a section or sections within a delay line is controlled via a secondary low-speed dual-direction delay-line. This secondary delay line is adjusted via a conventional phase-detector, and functions primarily as a dual-direction shift register, but may have a small number of stages which maintain analog voltages between digital equivalents. The mixed-signal control bits/nets can partially switch small capacitances onto the primary delay-line, adjusting the delay in arbitrarily small increments. This approach performs the low-pass filtering required in either analog or digital DLLs/PLLs, yet is smaller, and more power efficient than either. It also prevents the jitter in the output of digital DLLs/PLLs caused when the delay line control switches between distinct digital states. Further, it can be implemented entirely with conventional digital logic, making it attractive for use in integrated circuits/systems wherever synchronization and clock multiplication are necessary.

Patent Application

of

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for

8 Industrie Canada OPIC Industry Canada CIPO 8

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Remis à Chargé à

METHOD AND APPARATUS FOR MIXED-SIGNAL DLL/PLL AS USEFULL IN TIMING MANIPULATION

of which the following is a specification:

FIELD OF THE INVENTION

The present invention relates to integrated circuits, and more particularly, to those circuits which manipulate the delay of signals travelling within an integrated circuit or system.

BACKGROUND OF THE INVENTION

Delay-locked loops (DLLs) and phase-locked loops (PLLs) are commonly used to manipulate the delay through a circuit to match some reference period. Such circuits can then be easily extended to produce output clocks at rational multiples of a reference frequency: DLLs and PLLs are found in clock distribution networks, on-chip clock generators, synchronizers, clock-data-recovery systems, clock multipliers, de-skew circuits, etc... These circuits can be implemented in analog or digital form, where the primary complexity of the design is within the loop-filter which stabilizes the delay in the midst of speed-up (up) or slow-dn (dn) signals from a phase-error detector.

In analog implementations, the up/dn signals from a phase-detector feed a charge-pump which adds or removes charge from a large capacitance while the error signal is asserted. The voltage on the capacitance then adjusts the delay through the circuit to compensate and reduce the phase error. For singular up/dn signals, the voltage should have negligible change and thus it requires many subsequent commands to appreciably affect the delay. The main drawback with analog DLLs and PLLs is in the relatively large lock-time, area, power, and design time requirements of the loop filter and delay-line or oscillator.

In digital implementations, whenever an up/dn signal is asserted, it increments or decrements a counter within the digital control loop. It is important to note that, unlike analog charge-pumps, the width of the up/dn signal is not taken into account, and thus small and large phase errors are treated equally. The results from the counter are then digitally filtered and decoded into a large number of control bits (either logical 1 or 0) which abruptly switch the delay of the circuit. This abrupt switching leads to quantization induced jitter which degrades the quality of the output signal and can lead to functional errors. Digital filters also suffer from a relatively large power and area overhead, though their design and integration are much easier than their analog counterparts. Another

advantage of digital architectures is that the delay of the circuit is uniquely controlled by the digital control string which is usually stored in a set of registers. Since the lock-state of the circuit is in memory, portions of the system can be powered down without loss of timing alignment.

It should also be noted that hybrid solutions exist which use digital control loops for coarse locking and analog control loops for fine adjustment. This allows for relaxation of both the digital and analog filter requirements, but each of the two sub-loops still retain their inherent disadvantages of power, area, and integration inefficiency. In this case the outer digital control loop normally requires little filtering, and thus the complexity of such systems is normally dominated by the inner analog control loop.

This invention implements an analog filter, but constructed of a set of digital tri-state buffers. The circuit's digital features ease integration, extend lock range, permit fast lock, and allow for the circuit lock-state to be remembered, while its analog properties eliminate quantization induced jitter and allow significant reduction in area and power consumption over competing implementations.

	Analog	Digital	Hybrid	This Work
Power	High	High	High	Low
Area	High	High	High	Low
Noise	Low	High	Medium	Medium
Lock-time	High	Medium	Low	Low
Lock-range	Low	Medium	High	High
Power-down mode	No	Yes	No	Yes
Integration Cost	High	Low	High	Low

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1: A simplified overview of a particular embodiment of invented mixed-signal method and apparatus in a DLL configuration
Figure 2: Conventional analog delay locked loop
Figure 3: Conventional analog phase locked loop
Figure 4: One implementation of a voltage controlled delay line (VCDL)
Figure 5: Conventional digital delay locked loop
Figure 6: Conventional digital phase locked loop
Figure 7: Various conventional implementations of a digital delay element
Figure 8: Conventional dual loop PLL with digital outer loop and analog inner loop
Figure 9: A particular embodiment of the invention in a DLL configuration

SUMMARY OF THE INVENTION

The principle object of this invention is to provide a highly efficient implementation of a DLL/PLL such that it can be more extensively employed in integrated circuits.

Accordingly, more abundant use of an efficient DLL/PLL can lead to reduced power dissipation, area consumption and electromagnetic interference in other system components.

An associated object of the invention is to reduce the power consumption of the DLL/PLL compared to alternative implementations.

An associated object of the invention is to reduce the circuit area consumed by a DLL/PLL.

An associated object of the invention is to increase the digital delay resolution within the delay element(s) of a DLL/PLL.

An associated object of the invention is to provide a state memory for the control of a delay element within the DLL/PLL, this is contrary to analog DLLs/PLLs but is consistent with digital implementations.

An associated object of the invention is to eliminate quantization induced jitter which is dominant in digital DLL/PLL implementations.

An associated object of the invention is to increase the ease of integration of a DLL/PLL compared to analog implementations.

An associated object of the invention is to provide for a DLL/PLL with very wide-range tuning ability.

In accordance with these objects, a brief description of one embodiment of the invention is described:

In this method and apparatus, the delay of an element is controlled via a string of bits, similar to a digital DLL, but some of those bits may take on stable intermediate analog values between logical 1 and 0. Each control bit is connected to the gate of a transistor which effectively switches more or less capacitance onto the primary delay line, and therefore, modulates the delay through the circuit. The string of control bits is easily generated by a secondary low-speed dual-direction delay-line, which can be implemented using conventional digital tri-state inverters. Fed by a phase-detector, this line functions as a pseudo-thermostat coded, asynchronous dual-direction shift register. When up is asserted, the control bits shift slowly to the right, reducing capacitance on the primary delay-line. Alternately, when DN is asserted, bits shift leftwards, increasing the effective capacitance and slowing the circuit. Given slowly performing tri-states, the control string will often end in intermediate states between digitally defined values, and thus the circuit can settle into an arbitrary delay between any two digital control strings.

In this case, an analog loop filter is inherently formed from the distributed resistances and capacitances of the digital tri-state gates and loads. Though it is in essence an analog filter, because it is formed from a distributed set of standard digital cells it is small, power

efficient, and easily designed and integrated. As a result, the circuit requires no digital filter and can prevent quantization induced jitter. Also, though the filter is inherently analog, it retains the primary advantage of the digital DLL/PLL implementations in that the mostly digital control string can be stored and recalled. This allows the circuit to maintain lock (to within a margin of error) when the input is powered down, thus preventing the need for re-acquisition when a circuit is re-enabled.

DETAILED DESCRIPTION OF THE DRAWINGS

PRIOR ART

Figure 2 depicts a conventional analog delay locked loop, including conventional circuits for its implementation including a phase-detector 13, charge-pump 20, loop filter 21, a voltage controlled delay line (VCDL) 22, and optional edge combination circuit 24. Within the VCDL there may exist a number of adjustable delay elements 23 which are controlled by the output of the loop filter 21.

The phase-detector 12, detects the phase difference of the reference signal 13 versus the fed-back output signal 14 of the VCDL 22. If the output signal 14 arrives too early, ie. less than one clock period after the reference signal 13, it asserts the DN signal to increase delay through the VCDL 22, whereas if it arrives to late, it asserts the UP signal to lower the delay through the VCDL 22. In this manner, the delay through the VCDL 22 will be adjusted to match the period of the reference signal 13.

To control the delay adjustment, the analog delay locked loop uses an analog charge pump 20 and loop filter 21. The charge pump 20 is responsible for providing charge to the loop filter 21 for the duration of an UP signal, and extracting charge during a DN signal. It is normally carefully biased to ensure that the current supplied or extracted to the loop filter is nearly constant for the duration of the control signal. This leads to biasing arrangements that decrease the circuit's complexity and power efficiency. The output of the charge pump feeds an analog filter arrangement 21. Though Figure 2 shows only a simple RC based filter arrangement, other more complex analog filters may also be used. The role of the loop filter 21 is to average the effects of the UP/DN control signals to provide stability and ensure no sudden changes in the delay of the VCDL 22. It is typical that the die area of this loop filter 21 is the dominant cost in the manufacture of the DLL. The output of the loop filter 21 is an averaged analog voltage that controls all of the delay elements 23 within the VCDL 22.

Provided the reference period 13 is within design limits, once the system has had an opportunity to stabilize, the delay through the VCDL 22 will match the reference period 13. Given that each delay element 23 within the VCDL 22 is designed to match each other, the signal at various points in the VCDL 22 can be extracted with predictable phase relationship. For example, in Figure 2, with 4 delay elements 23 in the VCDL 22, the signal is extracted at 90 180 270 and 360 degrees. Combining these 4 clock phases can create an output clock at 4x the reference frequency.

Figure 3 outlines a conventional analog phase locked loop (PLL). Though most components of the DLL and PLL are similar, the phase locked loop has a controlled oscillator 25 whereas the DLL only contains a controlled delay line. In Figure 3, the ring-oscillator is formed using an odd number of inversion stages 23 within the VCDL 25. Other conventional PLLs use other forms of voltage-controlled oscillators (VCOs) in place of the VCDL based ring oscillator 25 shown. The PLL allows for simpler clock multiplication by placing a divider 26 in the feedback path to the phase-detector 12. Since the phase-detector 12 will adjust the charge-pump 20 and loop filter 21 until its inputs match, the actual frequency within the oscillator will be N times the reference frequency. The primary disadvantages of the PLL however, is that noise accumulates in the system with each cycle of the oscillator, whereas in a DLL, each edge of the reference clock 13 resets the system to its ideal state. A further disadvantage is that the loop filter 21 of the PLL must be designed to ensure stable operation whereas the DLL is unconditionally stable.

Figure 4 illustrates one conventional implementation of a voltage controlled delay line as may be used in the VCDLs 22 or 25 of the analog DLL or PLL. In this case the control voltage is used to control a number of current sources 27, which limit the amount of current, and hence the speed, of each cell 23 of the VCDL (22 or 25). Though the circuit is efficient in terms of area, it requires careful control of the cells 23 so that they have matching delay characteristics.

Figure 5 shows the conventional digital delay locked loop. In contrast to the analog DLL in Figure 2, the charge-pump and loop filter are replaced by an UP/DN counter 20, and digital filter 31. In most conventional digital DLLs a decoder 32 is also required to convert the output of the digital filter into a string of bits 33 that are appropriate for controlling the digital delay elements 35 within the digitally controlled delay line 34. In the case of the digital DLL, a long control string of digital bits controls the delay through the elements 35, as opposed to an analog DLL where a single well controlled analog voltage controls each element. As was the case in the analog DLL, an edge combination circuit 24 can be applied to generate an output clock at some multiple of the reference frequency. Though the digital DLL can be integrated more easily than an analog DLL, the digital filter and control logic tend to consume as much die area and power as the analog charge-pump 20 and loop filter 21 of Figure 3. Further, since each element 35 of the delay line 34 can take on only quantized values of delay, the overall delay through the line 34 fluctuates between discrete steps, leading to an output clock with poor jitter characteristics. It should be noted that some improvements of the conventional digital DLL include a preliminary thermometer coded shift register prior to the UP/DN counter 20. This shift register requires that a consecutive number of UP or DN signals be asserted before having any affect within the digital filter and thus slightly relaxes the digital filter requirements.

As was the case with the analog DLL, the conversion of a digital DLL to a PLL is straightforward by feeding the output of the oscillator directly back to its input. This is shown in Figure 6 where a numerically controlled ring oscillator is created by ensuring an

odd number of inversion stages 36 around the oscillator feedback loop. As with the analog PLL, the disadvantage of the digital PLL is the accumulation of noise and the possibility of instability.

Figure 7 illustrates five conventional implementations of the digitally controlled delay element 35. Implementation 43 is most commonly used since it is easily characterized and can be implemented with standard digital cells. Other conventional approaches either change the effective drive strength of the digital gate (40, 41, 44) or switch extra capacitive load onto the driven node (42). Each of these techniques are subject to various inefficiencies with respect to either area, power consumption, or resolution.

A final illustration of prior art is shown in the dual-loop PLL architecture of Figure 8. In this case a digital outer loop is used to provide coarse control before handing off fine control delay to an analog inner loop. Many variations on this theme exist which may consist of more than 2 loops, and different combinations of digital and analog control, filtering and delay elements. The common element between them however is that the digital control sections are purely digital, whereas the analog control sections are purely analog.

FIRST EMBODIMENT

Figure 1 shows a particular example of the invention used in a DLL configuration to produce a period-delay buffer. Though it is not the most practical embodiment of the invention, it serves to most easily illustrate the core principles.

The example illustration consists of a phase-error detector 12, the invented asynchronous dual-direction mixed-signal thermometer coded shift register 1a, novel mixed-signal variable delay line 11a, and a conventional buffer tree 15. The phase-error detector can be of any conventional form provided that the output correction signals UP and DN are mutually exclusive. The dual-direction shift register 1a is constructed using a set of tri-state buffers 2a connected in two serial chains. One chain of buffers 16a is responsible for sequentially discharging the control nets 4 in order to reduce the delay through the delay line 11a, whereas the other chain of buffers 17a, is responsible for sequentially charging the control nets to increase the delay through the delay line 11a. Further, the mixed-signal variable delay line 11a consists of any conventional driver cell 9, and a set of drain-connected transistors 7 where the source of the transistor is left physically unconnected. Left unconnected, the source of the transistors 7 will naturally form a small parasitic capacitor to the substrate 18 which is used along with the control nets 4 to regulate delay.

To illustrate the operation of the dual-direction shift-register 1a, consider the example timing diagram in Figure 1. First assume the phase-detector asserts the DN signal. In this case the set of buffers 17a will be enabled and sequentially charge control net_0, followed by control net_1, control net_2 and finally control net_3. If, on the next cycle the UP signal is asserted, control net_3 discharges, causing control net_2 and then control net_1 to begin to discharge. Once the UP signal is de-asserted however, the drivers will be

disabled and the nets will maintain their values – where in the example case, control net_1 and control net_2 stabilize at a voltage other than VDD (logical 1) or VSS (logical 0). Further application of the UP or DN signals from the phase-detector will cause the values on the control-nets to slowly vary and shift in order to reduce or increase the delay through the voltage controlled delay line 22. Though persistent application of either of these signals will cause the dual-direction shift-register to its limits at 1111 or 0000, in normal operation the control nets will settle to an intermediate value, where the majority of nets are at their digital extremes and a small number maintain analog values, fluctuating between VDD and VSS.

This string of mostly digital bits is then used to manipulate the delay through the VCDL 11a. Each control net is connected to a transistor which acts as an analog switch. As the control net voltage increases, extra capacitance is effectively exposed to the loaded net, thus slowing the signal progress. As the control net voltage lowers, the capacitance has less effect on the load and delay through the VCDL 11a decreases. In contrast to the conventional switched loading delay cell 42 of Figure 7, the switch does not use does not use a transmission gate and the control net is mixed-signal in nature, not passing through any logic which would cause undue power dissipation. Further, the characteristic of such a delay element is monotonic, where the delay varies predictably as the control voltage fluctuates between digital extremes VSS and VDD.

Another note of importance concerns the practical implementation of the adjusting switches 7 and connected capacitance 18. In actual embodiments of the invention there is normally no external capacitance 18 attached to the analog switch. The parasitic drain capacitance of the switch actually forms the small capacitance that is typically appropriate for fine control of the delay elements, and thus eliminates the need for extra capacitive components and wiring. This makes the parasitic control switches very efficient to implement in their physical layout and significantly reduces integration complexity.

SECOND EMBODIMENT

Figure 9 illustrates a more practical embodiment of the invention. In this case the dual-direction asynchronous shift-register is constructed of invertors 2b, rather than buffers. In this case, alternate control nets are attached to either PMOS or NMOS transistors to appropriately control delay.

Further, a more typical application of the invention would use a larger number of control cells ($2 < N < 1024$) rather than the 4 shown in Figure 1.

Also, depending on the application requirements, the number of adjustable delay stages 6, buffers 9, and switched capacitances 7/8 will vary significantly.

Further, optional latches 5 may be attached to each control net in order to store the closest digital representation of the delay-line setting. Such memory is useful to provide for extended power-down modes and quick reacquisition time. These latches can be made

using either conventional CMOS techniques or using two back to back tri-state buffers with slightly offset control signal timing.

A different approach to store the digital representation of the control nets is to make use of the back to back tri-states which already exist in the dual-direction asynchronous shift register 1b. By appropriately sectioning the UP/DN control signals and selectively turning on back-to-back drivers, the control nets will go to and store values close to their nearest digital representation. Though this approach adds very little circuitry to the design, it decreases the precision of the saved values since each pair of control nets are forced to complementary values.

A further enhancement shown in Figure 9 is the addition of extra capacitance 10 onto the control nets. The filtering qualities of the circuit are dependent on the drive strength of the tri-state buffers 2b and the capacitance on the control nets. Though in some applications the natural speed of the tri-states coupled with the parasitic capacitance of the wiring and gate-capacitance of the switches will be slow enough to provide necessary filtering, it may be necessary to decrease the drive strength and/or increase the capacitance to slow the charge and discharge times to acceptable values. This can be accomplished by using degenerate transistor sizing (where Width/Length ratios are < 1) and/or by adding extra capacitance to the control nets in the form of standard cell loads.

ENHANCEMENTS

It is possible to enhance the delay line 11 by modifying the drivers 9 to also have a variable drive strength or delay using any of the conventional methods (some of which are shown in Figure 4 and Figure 7). The control of these drivers 9 can then be controlled using another control loop. Such a control loop may be either analog, digital, or use the same dual-direction asynchronous shift register as described in this invention. If using this circuit in any configuration where the invented circuit is used for fine control, initial rough lock should be performed with the control nets 4 initialized to an intermediate value between the two extremes. This can be done with simple control logic on the UP/DN signal lines that divides the dual-direction shift register into two halves and on reset, asserts the UP control to one half and the DN control to the other half.

The phase-detector 12 may be constructed such that it can recognize a false-lock condition and provide the UP/DN control signals as appropriate.

The dual-direction asynchronous shift register can be used independently from the invented mixed-signal adjustable delay element in appropriate applications.

The mixed-signal switch transistors 7/8 may have an attached external capacitance in addition to its parasitic source capacitance. This will increase the range at the cost of lowered digital precision.

The sizing of the switch transistors 7/8 can be optimized to produce specific loop and filter characteristics.

The sizing of the effective delay capacitances 18 or switch transistors 7/8 can be manipulated to produce non-linear delay characteristics versus control word values.

The delay line 11 can be implemented in various other forms, including but not limited to those of Figures 4 and 7.

The delay line 11 can be implemented using differential circuitry.

The dual-direction asynchronous shift register can be implemented using any logic style (eg. CML, MCML, Dynamic logic, NMOS, ECL, etc..) or process (discrete, Si, SiGe, Ge, etc...)

The delay line 11 can be implemented using any logic style (eg. CML, MCML, Dynamic logic, NMOS, ECL, etc..) or process (discrete, Si, SiGe, Ge, etc...)

The invention can be used in a pair-wise configuration and applied to form a Vernier type delay line.

The invention can be applied to a voltage controlled oscillator where the control bits/nets are responsible for adjusting the resonance of the oscillator.

Added resistance or active circuitry may be placed between the tri-state drivers 2b and delay cells 6 to adjust the frequency response of the loop.

The asynchronous dual-direction shift register 1a may also be constructed using conventional asynchronous self-timed circuits rather than using the tri-state delay-line approach presented here. Such an approach would be a straightforward implementation of the method proposed here, but generally suffers from decreased circuit efficiency.

BENEFITS OF THE INVENTION

This invention significantly lowers the power consumption, integration complexity, area cost, design time and noise characteristics of delay based control systems/circuits. The resultant invention has specific application in delay-locked loop (DLL) and phase-locked loop (PLL) circuits. These circuits in turn can be used to provide clock recovery, phase synchronization, clock distribution, clock multiplication, clock synthesis, as well as in a host of other applications.

OTHER EMBODIMENTS

From the foregoing description, it will thus be evident that the present invention provides a design and method for the control of delay or oscillation based systems. Other embodiments will characteristically have the output of a phase or frequency detector feed a subsystem consisting of an asynchronous circuit to control the delay or oscillation frequency of a circuit. As various changes can be made in the above embodiments and operating methods without departing from the spirit or scope of the following claims, it is

intended that all matter contained in the above description or shown in the accompanying drawings should be interpreted as illustrative and not in a limiting sense.

CLAIMS

1. A delay lock loop circuit comprising:

- a phase detector receiving a reference signal and a feedback signal and having an UP output signal and a DOWN output signal;

- an asynchronous dual mixed signal shift register subcircuit receiving said UP output signal and said DOWN output signal;

- a delay line subcircuit having a plurality of delay elements and receiving said reference signal and outputs of said mixed signal shift register subcircuit, said delay line subcircuit producing said feedback signal;

wherein

- said shift register having a plurality of control nets, each control net producing one output of said shift register, each output of said shift register being coupled to one of said plurality of delay elements in said delay line subcircuit;

- said UP output signal and said DOWN output signal affects said plurality of control nets to increase or decrease a delay in said delay line subcircuit;

- each delay elements has an associated capacitance which directly affects said delay through said delay line.

2. A circuit according to claim 1 wherein

- said mixed signal shift register comprises dual parallel lines of cascaded circuit elements, one of said dual parallel lines of cascaded circuit elements receiving said UP output signal and the other of said dual parallel lines of cascaded circuit elements receiving said DOWN output signal.

3. A circuit according to claim 2 wherein one line of said dual parallel lines is coupled to Vss and said other line is coupled to Vdd.

4. A circuit according to claim 2 wherein each one of said cascaded circuit elements produces an output of said shift register and is coupled to a specific one of said plurality of control nets.

5. A circuit according to claim 4 wherein each one of said cascaded circuit elements is a tri-state buffer.

6. A circuit according to claim 4 wherein each one of said cascaded circuit elements is an inverter.

7. A circuit according to claim 1 wherein each delay element contributes to a total delay through said delay line.

8. A circuit according to claim 7 wherein each delay element comprises at least one transistor.

9. A circuit according to claim 8 wherein the or each of said at least one transistor is a drain-connected transistor with a source lead which is physically unconnected.

10. A circuit according to claim 1 wherein at least one of said control nets is coupled to an auxiliary control net.

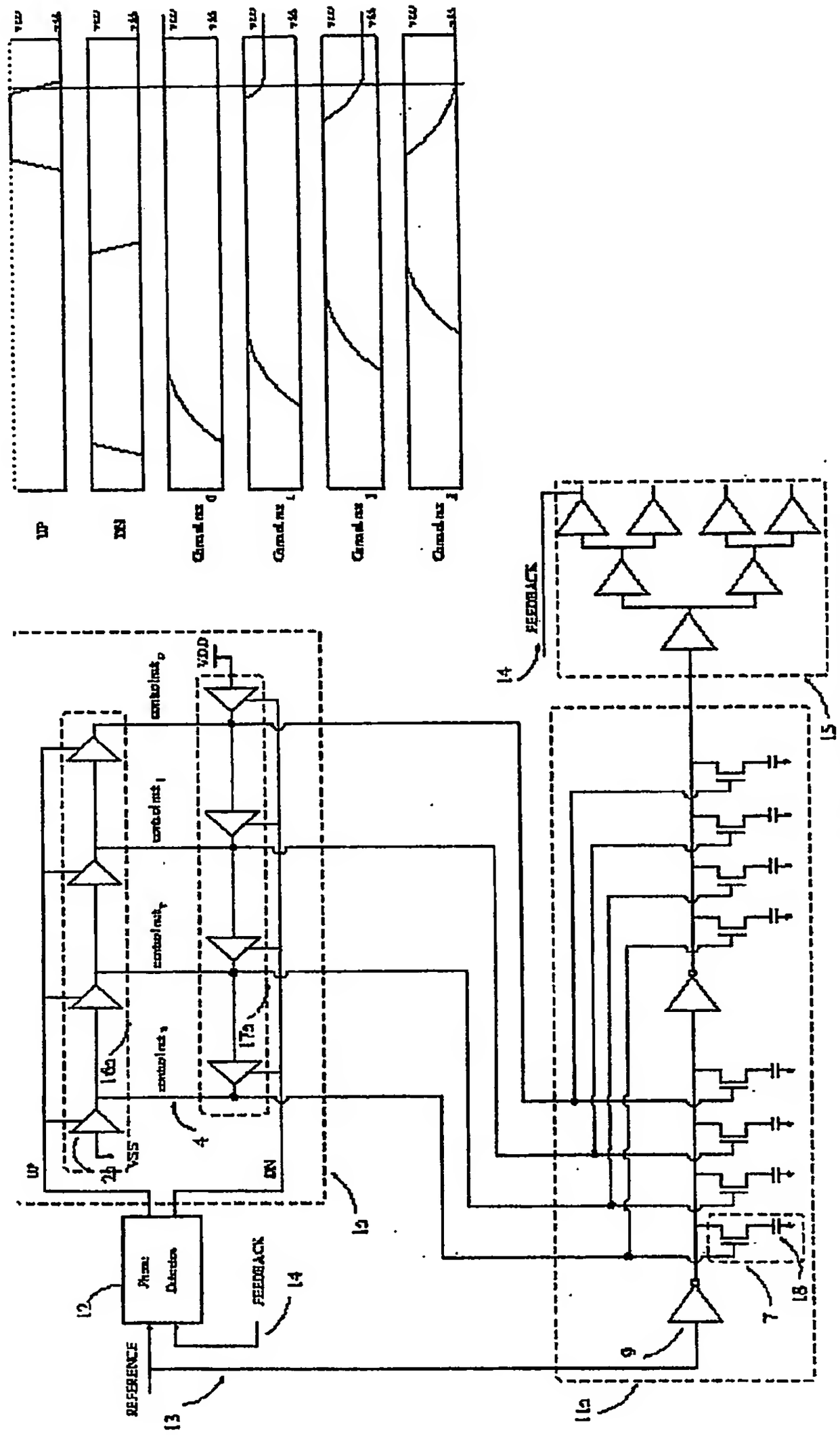

Figure 1: Simplified Overview of Invention

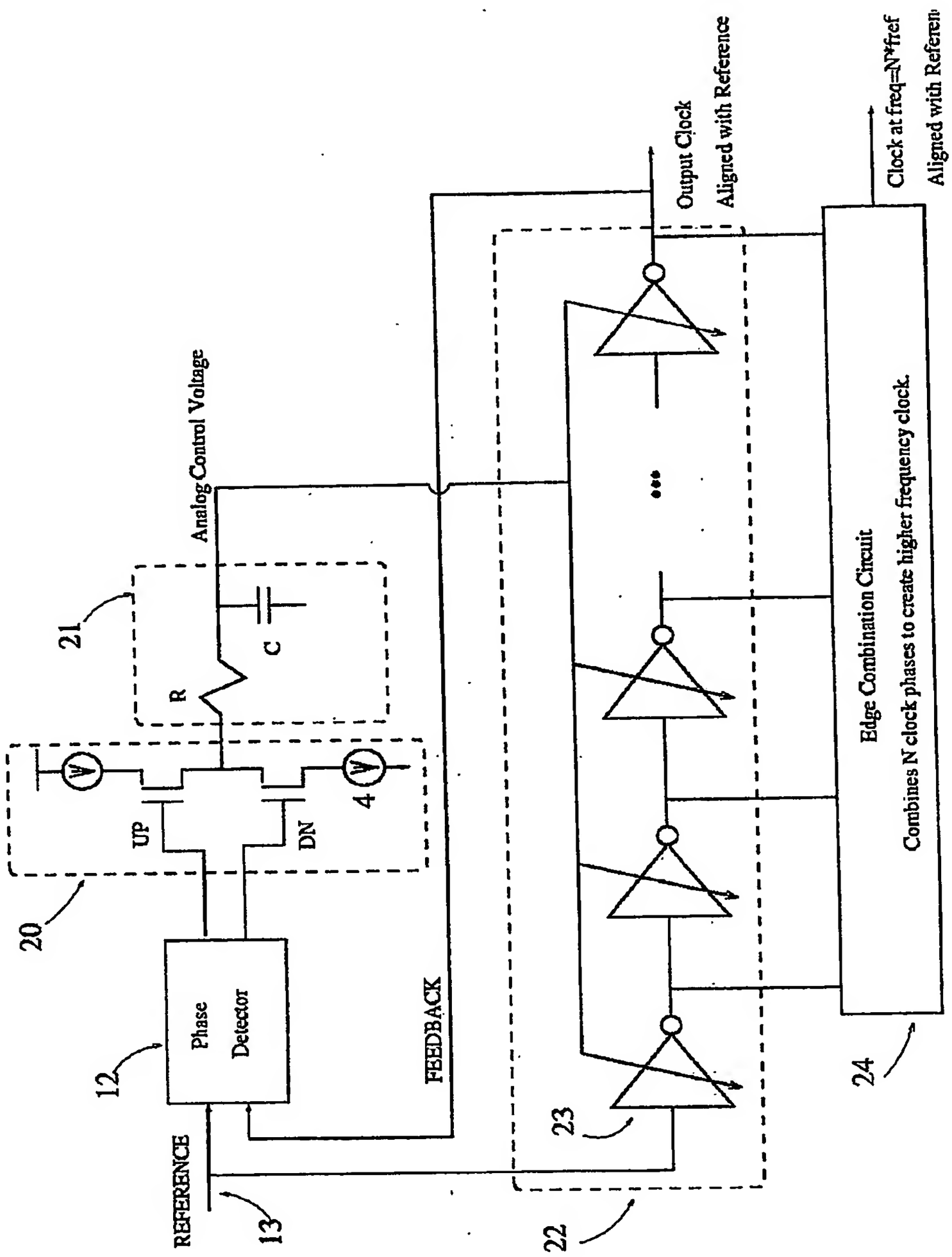

Figure 2: Conventional Analog Delay Loc

Locked Loop

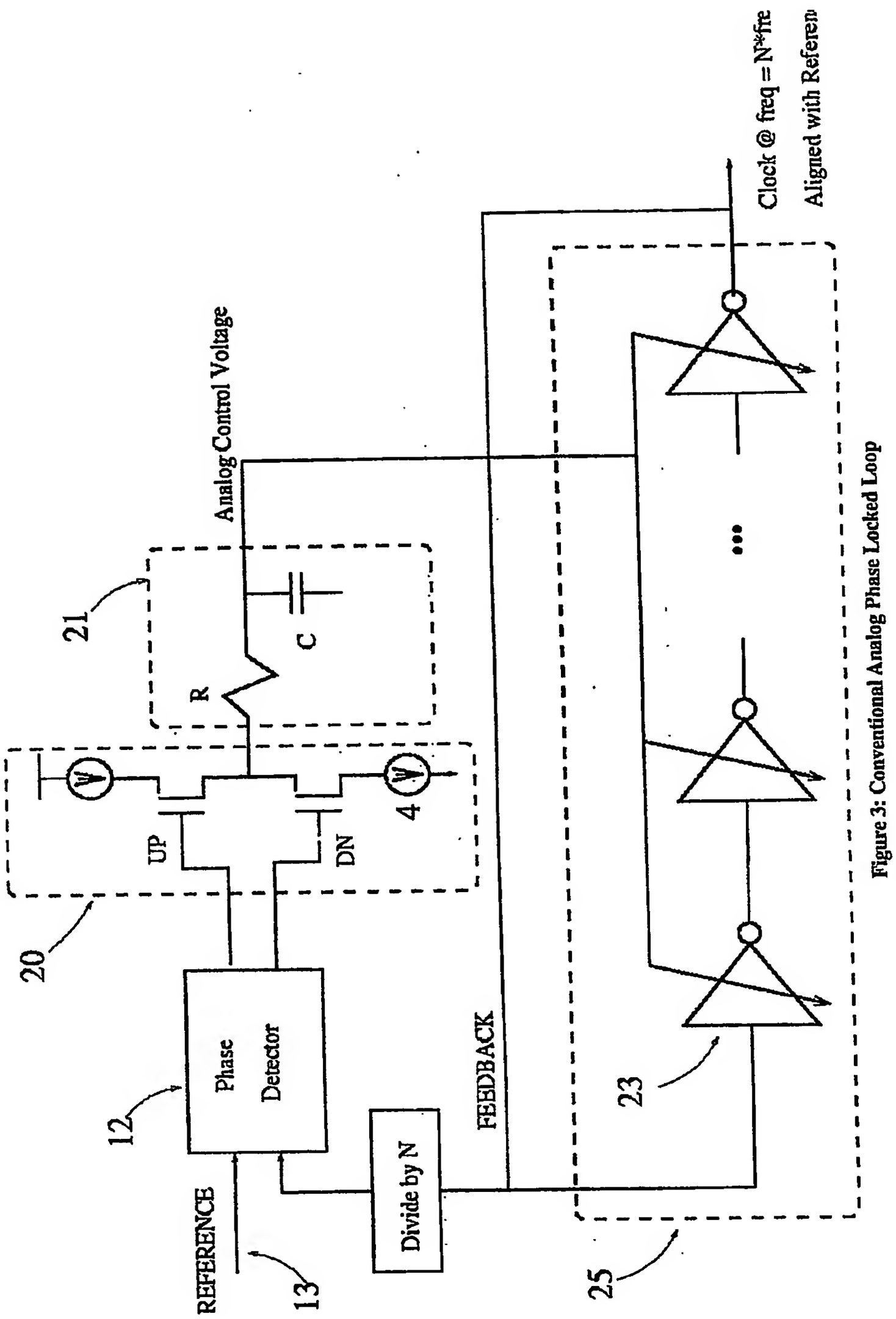

Figure 3: Conventional Analog Phase Locked Loop

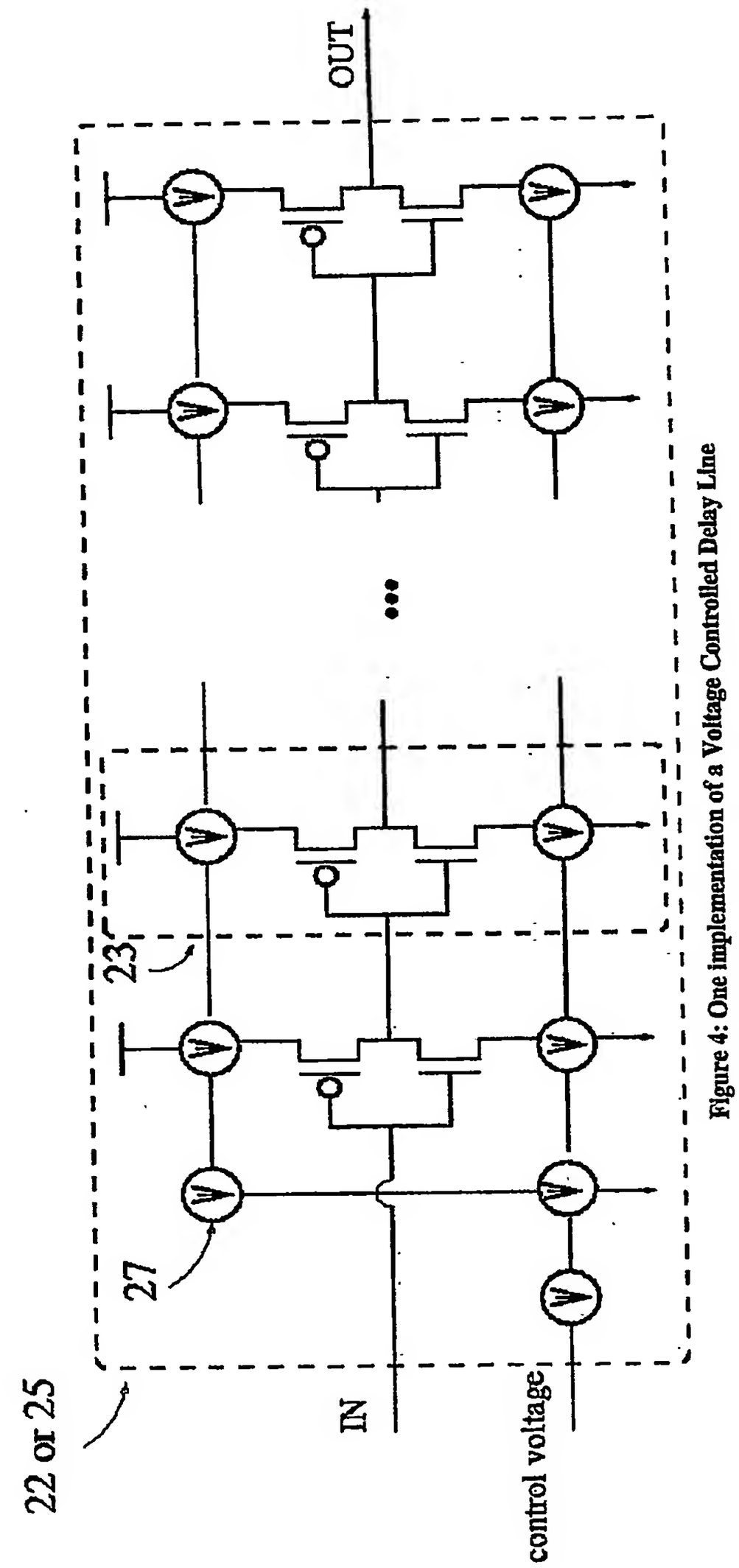

Figure 4: One implementation of a Voltage Controlled Delay Line

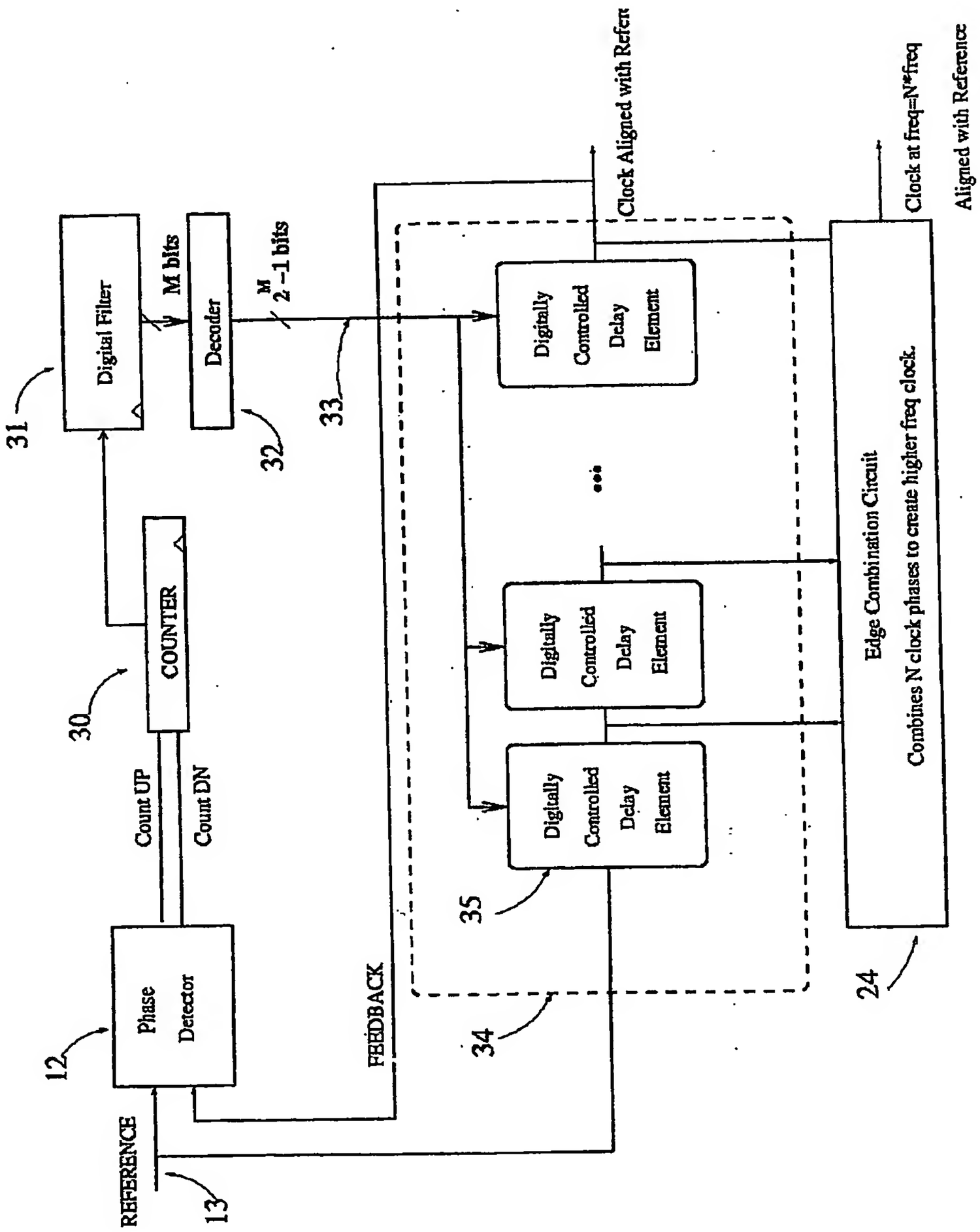

Figure 5: Conventional Digital Delay Locked Loop

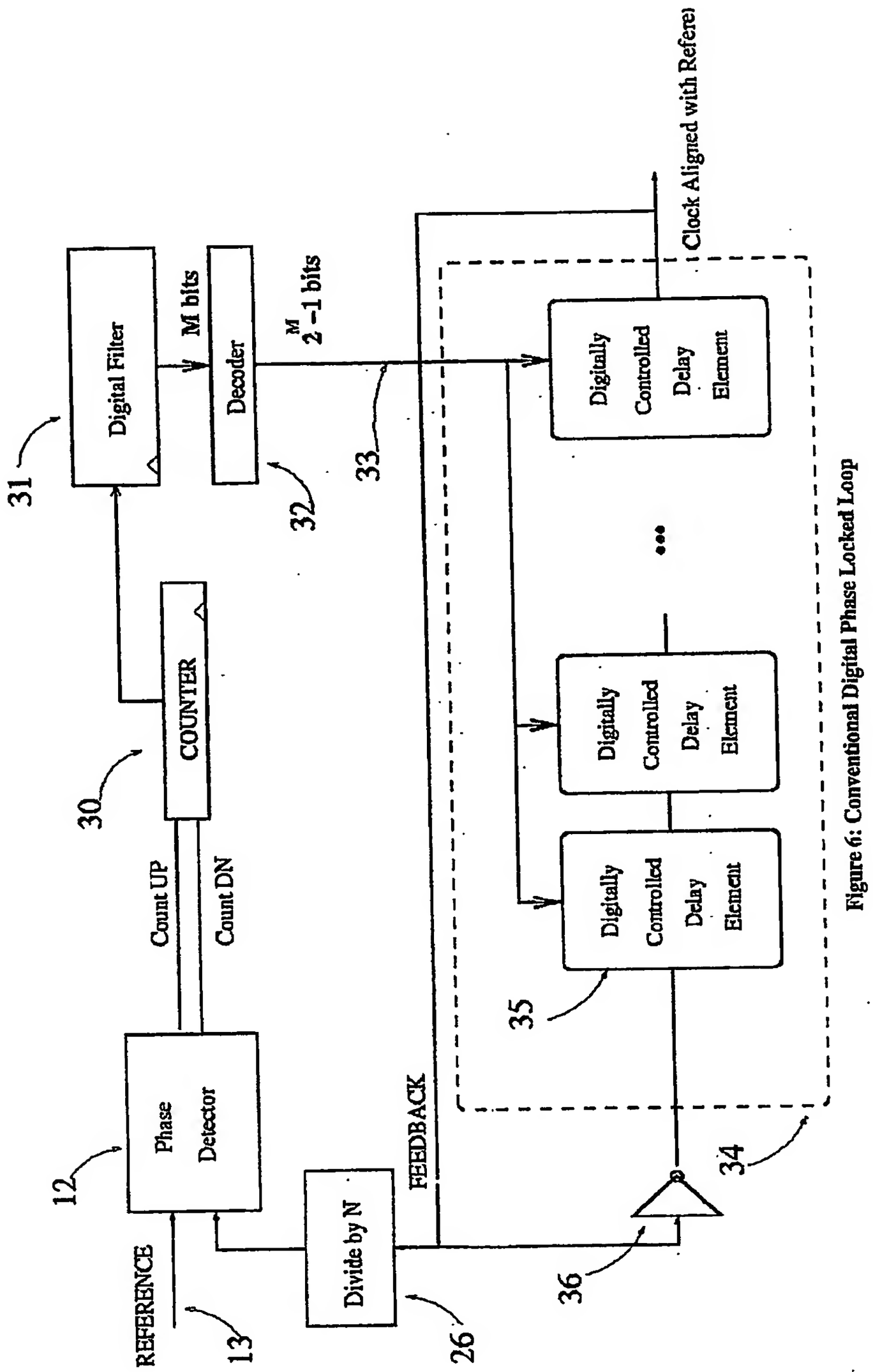

Figure 6: Conventional Digital Phase Locked Loop

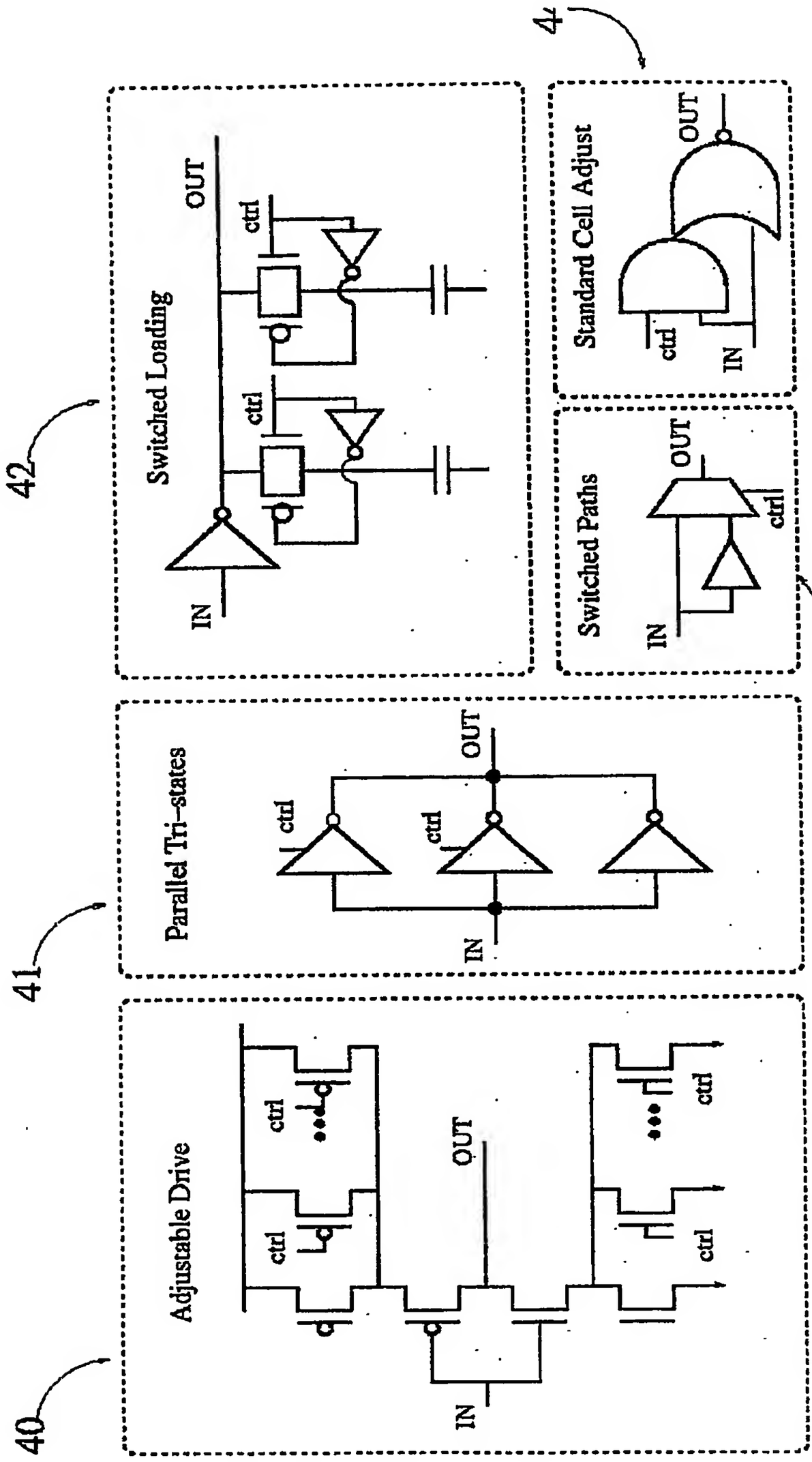

Figure 7: Various conventional digital delay elements